Replacement Abstract

A system for testing an embedded system containing a target processor executing a target program and target hardware that has a physical portion and a simulated portion. A target monitor determines when the target processor is attempting to access simulated hardware. The address bus of the microprocessor is monitored to detect an address in the address space of the simulated hardware. Lack of an acknowledge signal from the physical hardware within a predetermined period after the target processor attempts to access the target hardware may also indicate simulation. A bus capture circuit captures output signals on the bus connections of the target processor and converts the output signals to output data. The output data is then coupled through a communications interface to a hardware simulator. The hardware simulator processes the data in the same manner that the physical hardware would respond to signals corresponding to the output data.